ABSTRACT

A process of forming electrical interconnects between memory bits in a magnetoresistive memory device. A dielectric layer is formed to overlie a semiconductor substrate. A magnetoresistive storage layer is formed over the dielectric layer. An electrically conductive stop layer that is selective to etch processes and is mechanically hard is deposited over the magnetoresistive layer. A hardmask layer is formed to overlie the stop layer. The hardmask layer is etched to expose the stop layer. The stop layer and the magnetoresistive layer are etched using ion milling until the initial dielectric layer is exposed, defining individual magnetoresistive memory bits. A dielectric layer is formed over the hardmask layer and in the etch regions between magnetoresistive bits. The dielectric layer is planarized using chemical mechanical polish (CMP) until the stop layer is exposed. An interconnect layer is then formed over the exposed regions of the stop layer and is etched to form electrical interconnects between memory bits.